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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/963,590	09/27/2001	Mitsuru Komiyama	F00ED0023	9688

26071 7590 06/03/2004

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EXAMINER	
GRAYBILL, DAVID E	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 06/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/963,590	KOMIYAMA ET AL.	
	Examiner	Art Unit	
	David E Graybill	2827	

-- The MAILING DATE of this communication app ars on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 March 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 September 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the features of claims 3, 4, 17 and 18 must be shown or the features canceled from the claims. No new matter should be entered. To further clarify, the drawings do not show the claimed process limitations including "preformed," "as a beginning connection" and "as an ending connection."

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

In the rejections infra, generally, reference labels are recited only for the first recitation of identical claim elements.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 13, 14, 19-23, 25, 26, 28, 31, 32, 35 and 36 are rejected under 35 U.S.C. 102(b) as being anticipated by Takiar (5422435), or in the alternative, under 35 U.S.C. 103(a) as obvious over Takiar (5422435) in combination with Fujishima (6148505).

At column 4, line 42 to column 8, line 51, and column 10, lines 57-61, Takiar discloses the following:

A multi-chip package type semiconductor device, comprising: a first semiconductor chip 22 having a first terminal pad 32 and a conductive relay pad 58, the conductive relay pad including a first area (any portion of the total area of the pad 58) and a second area (the portion of the total area of the pad 58 other than the first area) which is different from the first area, a second semiconductor chip 24, which is placed on the first semiconductor

chip, the second semiconductor chip having a second terminal pad 54, connected (electrically and at least indirectly physically) to the conductive relay pad in the second area; a first internal terminal 46 connected to the first terminal pad; and a second internal terminal 44 connected (electrically and at least indirectly physically) to the conductive relay pad in the first area; an insulating substrate "carrier member," wherein the first and second internal terminals are formed on the insulating substrate, and the first semiconductor chip is placed on the insulating substrate, wherein the first area and the second area are inherently located along a side of the first semiconductor chip; a plurality of first terminal pads and a plurality of conductive relay pads, wherein each first terminal pad and each conductive relay pad are inherently alternatively aligned, wherein the first terminal pad is rectangularly-shaped, and a side of the first terminal pad is parallel to the side of the first semiconductor chip.

A multi-chip package type semiconductor device, comprising: a first semiconductor chip having a first conductive portion 32 and a second conductive portion 58, the second conductive portion having a first area and a second area, which is different from the first area; a second semiconductor chip, which is placed on the first semiconductor chip, the second semiconductor chip having a third conductive portion 54, connected to the second conductive portion in the first area; a first internal terminal

connected to the first conductive portion (column 6, lines 15-18); and a second internal terminal connected to the second conductive portion in the second area, wherein the first area and the second area are located along a side of the first semiconductor chip; an insulating substrate, wherein the first and second internal terminals are formed on the insulating substrate, and the first semiconductor chip is placed on the insulating substrate; a plurality of first conductive portions and a plurality of second conductive portions, wherein each first conductive portion and each second conductive portion are inherently alternatively aligned, wherein the first conductive portion is rectangularly-shaped, and a side of the first conductive portion is parallel to the side of the first semiconductor chip, wherein the first area and the second area are inherently spaced from each other.

A multi-chip package type semiconductor device, comprising: an insulating substrate; a first conductive pattern formed on the insulating substrate; a first semiconductor chip mounted on the insulating substrate; a second conductive pattern 58 formed on the first semiconductor chip, the second conductive pattern having a first area and a second area, which is different from the first area; a second semiconductor chip mounted on the first semiconductor chip; a third conductive pattern 54 formed on the second semiconductor chip; a first wire 56 connected (electrically and at least indirectly physically) between the first area of the second conductive pattern

and the third conductive pattern; and a second wire 60 connected (electrically and at least indirectly physically) between the second area of the second conductive pattern and the first conductive pattern, wherein the first area and the second area are located along the side of the first semiconductor chip, wherein the first area and the second area are inherently spaced each other.

To further clarify the disclosure of a first internal terminal 46 connected to the first terminal pad 32, it is noted that the terminal and pad are at least thermally connected and indirectly physically connected, and at column 6, lines 15-18, are further disclosed as connected by wire bonding.

To further clarify the disclosure of an insulating substrate "carrier member," it is noted that, as cited, Takiar discloses, "the phrase 'mounted on a carrier member' is intended to mean that a particular element (in this case the die 22) is either directly attached to the carrier member 42, or that the particular element is attached to some other structure or combination of structures, such as another element, stack of elements." Furthermore, as cited, Takiar discloses that the "element" is comprised of "dielectric [insulating] layers [that] can be either polyimide or SiO.sub.2, both of which are standard dielectrics in IC fabrication."

To further clarify the disclosure that the terminal pads and relay pads are inherently alternatively aligned, it is noted that, at column 6, lines 38-

50, Takiar discloses that there are alternative alignments other than the explicitly taught alignments. Therefore. it is inherent that the pads are aligned alternatively to the alternative alignments. Also, as illustrated in Figure 6, in the top row of pads, Takiar explicitly discloses terminal pads and relay pads alternatively (alternately) aligned.

Although inherent in the disclosures of Takiar, Takiar does not appear to explicitly teach the conductive relay pad including a first area and a second area which is different from the first area, the second terminal pad connected to the conductive relay pad in the second area, the second internal terminal connected to the conductive relay pad in the first area, the second conductive portion having a first area and a second area which is different from the first area, the third conductive portion connected to the second conductive portion in the first area, the second internal terminal connected to the second conductive portion in the second area, the second conductive pattern having a first area and a second area, which is different from the first area, the first wire connected between the first area of the second conductive pattern and the third conductive pattern, and a second wire connected between the second area of the second conductive pattern and the first conductive pattern.

Nevertheless, at column 4, line 36 to column 5, line 17, Fujishima discloses a conductive relay pad (P or 40) including a first area 41 and a

second area (41 or Pa) and a first (5 or 5a) and second (5 or 5b) wire connected to the first and second area, respectively. In addition, it would have been obvious to substitute the relay pad and wire connection of Fujishima for the relay pad and wire connection of Takiar because substitution of a known element based on its suitability for its intended has been held to be prima facie obvious. See MPEP 2144.07.

Claims 24 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Takiar and Fujishima as applied to claims 20 and 25.

As cited, Takiar discloses a first wire 60, the first wire having one end connected to the second terminal and the other end connected to the second conductive portion, wherein the first wire is connected to the first area and the second wire is connected to the third conductive pattern.

However, Takiar does not appear to explicitly teach the wires connected through bumps.

Nonetheless, at column 4, lines 1-39, Fujishima discloses wires 5 connected through bumps 53. Furthermore, it would have been obvious to combine the product of Fujishima with the product of Takiar because it would facilitate wire connection.

Claims 1, 2, 15 , 16, 29, 30, 33 and 34 are rejected under 35 U.S.C. 103(a) as obvious over Takiar (5422435), or Takiar (5422435) in combination with any of Haba (6376904) and Fujishima (6148505).

As cited supra, Takiar discloses the following:

A multi-chip package type semiconductor device, comprising: an insulating substrate having thereon a first conductive pattern 46 and a second conductive pattern 44; a first semiconductor chip having a first internal circuit on the insulating substrate, the first semiconductor chip having a first terminal pad connecting to the first internal circuit and a conductive relay pad isolated from the first terminal pad, and the conductive relay pad including a first area and a second area, which is different from the first area; a second semiconductor chip on the first semiconductor chip, the second semiconductor chip being smaller than the first semiconductor chip, and having a second internal circuit and having a second terminal pad connecting to the second internal circuit; a first bonding wire connecting the first terminal pad to the first conductive pattern; a second bonding wire 60 connecting (electrically and at least indirectly physically) the second conductive pattern to the conductive relay pad in the first area; and a third bonding wire 56 connecting (electrically and at least indirectly physically) the conductive relay pad in the second area to the second terminal pad; a plurality of first terminal pads and a plurality of conductive relay pads,

wherein each first terminal pad and each conductive relay pad are inherently alternatively aligned, wherein the first terminal pad is rectangularly-shaped, and a side of the first terminal pad is parallel to the side of the first semiconductor chip, wherein the second semiconductor chip is placed on the center of the first semiconductor chip.

A multi-chip package type semiconductor device, comprising: an insulating substrate having a first and second conductive patterns thereon; a first semiconductor chip on the insulating substrate, the first semiconductor chip having a first internal circuit, a first terminal pad connecting to the first internal circuit and a conductive relay pad isolated from the first terminal pad; a second semiconductor chip on the first semiconductor chip, the second semiconductor chip being smaller than the first semiconductor chip, and having a second internal circuit and having a second terminal pad connecting to the second internal circuit, a first bonding wire connecting the first terminal pad to the first conductive pattern; a second bonding wire connecting the second conductive pattern to the conductive relay pad; and a third bonding wire connecting the conductive relay pad to the second terminal pad; a plurality of first terminal pads and a plurality of conductive relay pads, wherein each first terminal pad and each conductive relay pad are inherently alternatively aligned, wherein the first terminal pad is rectangularly-shaped, and a side of the first terminal pad is parallel to the

side of the first semiconductor chip, wherein the second semiconductor chip is placed on the center of the first semiconductor chip.

To further clarify the disclosure that the terminal pads and relay pads are inherently alternatively aligned, it is noted that at column 6, lines 38-50, Takiar discloses that there are alternative alignments other than the explicitly taught alignments. Therefore, it is inherent that the pads are aligned alternatively to the alternative alignments. Also, as illustrated in Figure 6, in the top row of pads, Takiar explicitly discloses terminal pads and relay pads alternatively (alternately) aligned.

However, Takiar does not appear to explicitly teach wherein the lengths of the first, second and third bonding wire are approximately the same.

Nevertheless, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose these particular relative lengths because, as cited, Takiar discloses that wire bond length is a result effective variable, and applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the product would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the

limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); In re Dailey, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

In any case, at column 6, lines 6-12, Haba discloses wherein the lengths of first, second and third bonding wires 440a, 440b, 440c, respectively, are approximately the same. In addition, it would have been obvious to combine the product of Haba with the product of Takiar, because it would provide desirable electrical properties.

Although inherent in the disclosures of Takiar, Takiar does not appear to explicitly teach the conductive relay pad including a first area and a second area which is different from the first area, a second bonding wire connecting the second conductive pattern to the conductive relay pad in the first area; and a third bonding wire connecting the conductive relay pad in the second area to the second terminal pad.

Nevertheless, at column 4, line 36 to column 5, line 17, Fujishima discloses a conductive relay pad (P or 40) including a first area 41 and a second area (41 or Pa) and a first (5 or 5a) and second (5 or 5b) wire connected to the first and second area, respectively. In addition, it would

have been obvious to substitute the relay pad and wire connection of Fujishima for the relay pad and wire connection of Takiar because substitution of a known element based on its suitability for its intended has been held to be prima facie obvious. See MPEP 2144.07.

Claims 3-12, 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Takiar (5422435) and Fujishima (6148505), or the combination of Takiar (5422435), Haba (6376904) and Fujishima (6148505), as applied to claims 2 and 16.

As previously cited, Takiar discloses the following:

A multi-chip package type semiconductor device comprising wherein the first bond as the beginning connection of the first bonding wire is preformed at the first terminal pad and the second bond as the ending connection of the first bonding wire is made at the first conductive pattern, wherein the first bond as the beginning connection of the second bonding wire is preformed at the second conductive pattern and the second bond as the ending connection of the third bonding wire is made at the second terminal pad, wherein the first bond as the beginning connection of the first bonding wire is preformed at the first terminal pad and the second bond as the ending connection of the first bonding wire is made at the first conductive pattern, and the second bond as the ending connection of the second bonding wire is made at the second conductive pattern, and wherein

the first bond as the beginning connection of the third bonding wire is preformed at the second terminal pad, wherein the conductive relay pad is rectangularly-shaped (square), and is formed on the periphery of the first semiconductor chip, and a longer side (the top side in the length direction which is inherently longer than everything shorter than the longer side) of the rectangularly-shaped conductive relay pad is parallel to a side (the top side) of the first semiconductor chip, and a shorter side (the top side in the width direction which is inherently shorter than everything longer than the shorter side) of the rectangularly-shaped conductive relay pad is parallel to a side (the top side) of the first semiconductor chip, wherein the first area is electrically connected to the first bond of the third bonding wire via the conductive relay pad, wherein the second area is electrically connected to the first bond of the second bonding wire via the conductive relay pad, wherein the first bond as the beginning connection of the first bonding wire is preformed at the first terminal pad and the second bond as the ending connection of the first bonding wire is made at the first conductive pattern, wherein the first bond as the beginning connection of the second bonding wire is preformed at the second conductive pattern and the second bond as the ending connection of the second bonding wire is made at conductive relay pad, and wherein the first bond as the beginning connection of the third bonding wire is preformed at the conductive relay pad and the second

bond as the ending connection of the third bonding wire is made at the second terminal pad, wherein the first bond as the beginning connection of the first bonding wire is preformed at the first terminal pad and the second bond as the ending connection of the first bonding wire is made at the first conductive pattern, wherein the first bond as the beginning connection of the second bonding wire is preformed at the second conductive pattern and the second bond as the ending connection of the second bonding wire is made at the conductive relay pad, and wherein the first bond as the beginning connection of the third bonding wire is preformed at the second terminal pad and the second bond as the ending connection of the third bonding wire is made at the conductive relay pad.

It is noted that the product of Takiar inherently possesses the structural characteristics imparted by the process limitations of claims 3, 4, 17 and 18. See In re Fitzgerald, Sanders, and Bagheri, 205 USPQ 594 (CCPA 1980).

However, Takiar does not appear to explicitly teach that the wires are connected through bumps.

Nonetheless, at column 4, lines 1-39, Fujishima discloses wires 5 connected through bumps 53. Furthermore, it would have been obvious to combine the product of Fujishima with the product of Takiar because it facilitate wire connection.

Also, Takiar does not appear to explicitly teach the second bond is made at the first area, and wherein the first bond is preformed at the conductive relay pad in the second area; wherein the first bond of the second bonding wire is preformed at the conductive relay pad in the first area; and the second bond of the third bonding wire is made at the second area, wherein a distance from the side of the first semiconductor chip to the first area is almost the same as that from the side of the first semiconductor chip to the second area, wherein the first area is spaced apart from the first bond of the third bonding wire, wherein the second area is spaced apart from the first bond of the second bonding wire, wherein the first area of the rectangularly-shaped conductive relay pad is closer to a side of the first semiconductor chip than the second area.

Regardless, as cited supra, Fujishima discloses wherein a bond of a bonding wire (5 or 5a) is preformed at a conductive relay pad 40 in a first area, and another bond of another bonding wire (5, 5b) is made at a second area (41, Pa), wherein a distance from a side of a semiconductor chip to the first area is almost the same as that from the side of the semiconductor chip to the second area, wherein the first area is spaced apart from the another bond of the another wire, wherein the second area is spaced apart from the bond of the wire, and wherein the first area of the rectangularly-shaped

conductive relay pad is closer to a side of the semiconductor chip than the second area.

To further clarify the disclosure wherein a distance from a side of a semiconductor chip to the first area is inherently almost the same as that from the side of the semiconductor chip to the second area, wherein the first area is spaced apart from the another bond of the another wire, wherein the second area is spaced apart from the bond of the wire, and wherein the first area of the rectangularly-shaped conductive relay pad is closer to a side of the semiconductor chip than the second area, it is noted that the disclosure of Fujishima of the orthogonal relationship between the various relay pad configurations and the chip satisfies these limitations.

Furthermore, it would have been obvious to substitute the relay pad and wire connection of Fujishima for the relay pad and wire connection of Takiar because substitution of a known element based on its suitability for its intended has been held to be prima facie obvious. See MPEP 2144.07.

Applicant's amendment and remarks filed 3-10-4 have been fully considered, and are addressed supra and infra.

Applicant asserts that "the disclosure of Takiar, [at column 6, lines 15-18] is abstractive and ambiguous."

This assertion is respectfully traversed because this disclosure is not abstractive and ambiguous.

Also, applicant alleges, "as the examiner admitted, the Takiar does not disclose the electrical contact."

This allegation is respectfully traversed because the scope of the claims is not limited to an electrical contact, the prior art is not applied to the rejections for this disclosure, and there is no admittance in the record that Takiar does not disclose this unclaimed limitation.

In addition, applicant contends that the rejection provides no motivation to combine Fujishima and Takiar.

This contention is respectfully traversed because proper motivation to combine is elucidated in the rejection; namely, "it would have been obvious to substitute the relay pad and wire connection of Fujishima for the relay pad and wire connection of Takiar because substitution of a known element based on its suitability for its intended has been held to be prima facie obvious."

The remaining arguments merely assert that particular prior art references do not disclose particular limitations, yet, for which disclosures the particular references are not relied on. To this end, it is respectfully submitted that the rejection is not overcome by pointing out that one reference does not teach a particular limitation when the reference is not relied on for that teaching. In re Lyons 150 USPQ 741 (CCPA 1966). Moreover, it is well settled that one cannot show non-obviousness by

attacking the references individually where, as here, the rejection is based on combinations of references. In re Keller, 208 USPQ 871 (CCPA 1981); In re Young, 159 USPQ 725 (CCPA 1968).

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Any telephone inquiry of a general nature or relating to the status (MPEP 203.08) of this application or proceeding should be directed to Group 2800 Head SAE Linda Hodge-Taylor whose telephone number is 571-272-1585.

Any telephone inquiry concerning this communication or earlier communications from the examiner should be directed to David E. Graybill at (571) 272-1930. Regular office hours: Monday through Friday, 8:30 a.m. to 6:00 p.m.

The fax phone number for group 2800 is (703) 872-9306.

David E. Graybill
Primary Examiner
Art Unit 2827

D.G.
28-May-04